3A I²C Controlled USB/Adapter Li-ion Battery Charger with Power Path and 2.1A OTG Boost

Features

- 20V Input Voltage Tolerance, 3.9V–7V Operating Voltage Range
- High Efficiency 3A Switch Mode Charger
- USB-Compliant/Adapter Charger
  - USB1.0/2.0/3.0 Compliant Input Current Limit
  - 0.1-3A Programmable Input Current Limit
- Autonomous Preconditioning/CC/CV Charge Control, Termination and Recharge
- 1.5MHz Synchronous PWM Converter for Small 1uH Inductor
- USB OTG Boost Programmable Vout: 4.55 V - 5.51 V
  - Max Iout: 2.1A@4.55-5.51V
  - 90% Efficiency at 1.5A
  - Hiccup Mode Over-Current Protection for Reliable Capacitive Load Start-up
- Power Path Management
  - Instant System On with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Assistant Mode
- Full Range Programmable Charge Parameter through I²C Compatible Interface
- Accuracy (0°~125°C)
  - ±1% Charge Voltage Regulation
  - ±10% Charge Current Regulation
  - ±15% Input Current Regulation
  - ±2% Output Regulation in Boost Mode
- High Integration
  - Dynamic Power Path Management
  - Synchronous Switching MOSFET
  - Integrated Current Sensing
  - Bootstrap Diode
  - Internal Loop Compensation
- Comprehensive Protection
  - Safety Timer with Reset Control
  - Thermal Regulation and Shutdown
  - Input &Output Over-Voltage Protection
  - Output Over Current Protection
  - Reverse Battery Leakage Protection
- Charge Status Output for LED or Host Processor
- Shipping Mode and Low Battery Leakage Current
- 4mm X 4mm QFN-24 Package

Applications

- Tablet PC
- Smart Phone
- Power Bank
- Portable Media Player

Order Information

Part Number	HL7026
I^2C Address	6BH
USB Detection	PSEL
Default Battery Voltage	4.208V
Default Charge Current	2.048A
Max Charge Current	3A
Max Pre-charge Current	2.048A
OTG Current (Max)	2.1A
Charging Temperature Profile	Cold/Hot, 2TS pins
Status Output	STAT, PGN
STAT during Fault	Blinking@1Hz
Package	4mm X 4mm QFN-24
Packing Method	Tape & Reel

Typical Application Diagram

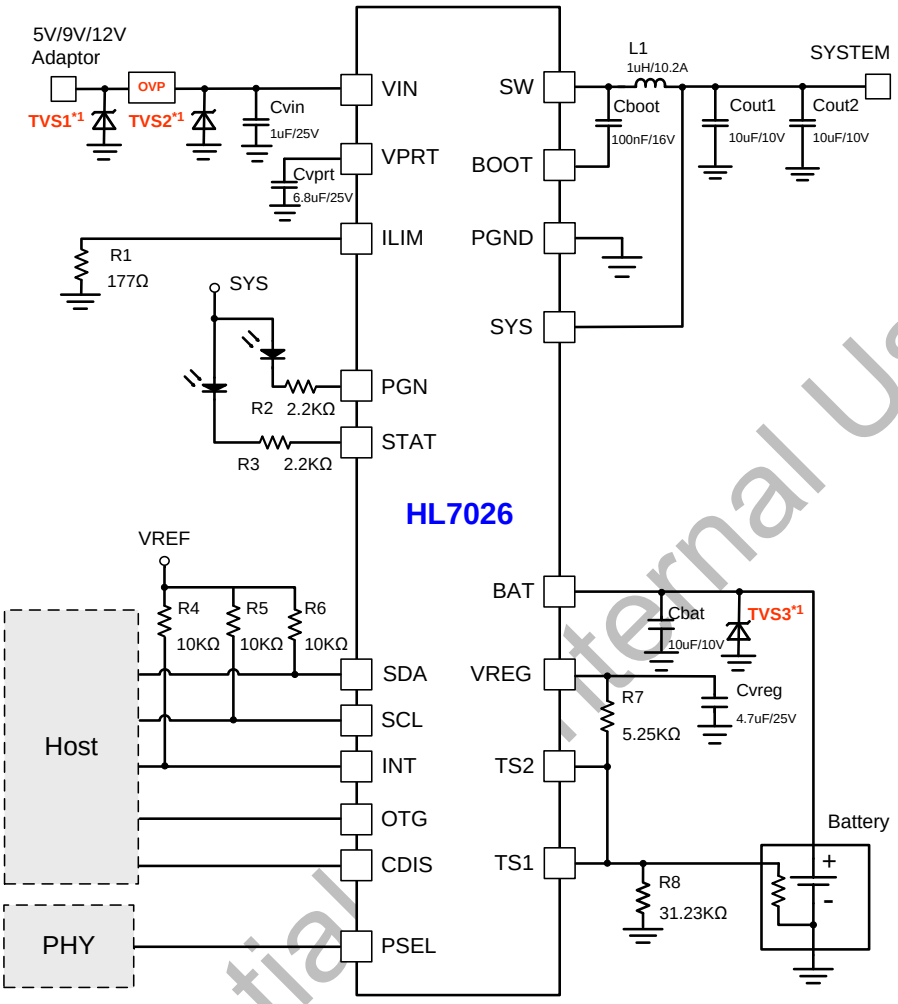


Figure 1 HL7026 Typical Application Diagram

Notice

***1**. Careful board level surge protection using TVS diode and OVP device on VIN pin, and TVS diode on VBAT pin, is essential to withstand high voltage spikes that may appear in PCB manufacturing process or end user applications. Without such protection, the IC is prone to electrical over-stress damage.

Component	Part Number	Value	Size	Vendor
L1	IHLP2020ABER1R0M01	1μH/10.2A	-	VISHAY
Cvin	CGA5L2X7R1E105K160AD	1μF/25V	1206	TDK
Cvprt	C3225X5R1E685K	6.8μF/25V	1210	TDK
Cboot	C0603X5R1C104K	100nF/16V	0603	TDK
Cvreg	C1206C475K3PACTU	4.7μF/25V	1206	KEMET
Cbat,Cout1,Cout2	C0805C106K8PACTU	10μF/10V	0805	KEMET
R1	-	177Ω	-	-
R2, R3	-	2.2kΩ	-	-

R4,R5,R6	-	10kΩ	-	-
R7	-	5.25kΩ	-	-
R8	-	31.23kΩ	-	-
TVS1/TVS2	See Table2	-	-	Will SEMI
OVP	See Table3	-	-	Will SEMI

Table 1 Recommended Component list

Component	Package	P_{PK}(W) tp=8/20 μs	Part Number	V_{RWM} (V)	V_F(V) I_F=20Ma		IR(μA)	V_{BR} (V)		
				Max	Min	Max	Max	Min	Typ	Max
TVS1	DFN2×2-3L	4000	ESD5641D12	12.0	0.45	1.25	0.1	13.0	15.0	17.0
TVS2	DFN2×2-3L	4000	ESD5641D07	7.5	0.45	1.25	1.0	8.0	9.0	10.0
TVS3	DFN2×2-3L	3500	ESD56161D04	4.5	0.50	1.10	8.0	5.1	5.7	6.3

Table 2 Recommended TVS

Component	Part Number	VIN(MAX)	RON	Package	Component Dimensions(mm)		
					L	W	H
OVP	WS3210C68	30V	45mΩ	WLCSP-9B	1.400	1.400	0.586

Table 3 Recommended OVP

Description

HL7026 is a fully integrated switch-mode Li-ion battery charger with power MOSFET, power path management, I²C interface and USB On-The-Go (OTG) boost function. It can be used with single cell or multiple-cell in parallel Li-ion and Li-polymer batteries in a wide range of smart phones, tablets, power banks and other portable devices. Its switch-mode operation and low-resistance power path maximize charging, discharging and boost efficiency, reduce battery charging time and extend battery life during the discharging phase.

This device supports a wide range of input sources, including standard USB host port, USB charging port and high power AC-DC adapter. It supports an input operating voltage from 3.9V to 13.2V, and can power up the system rail without a battery. It can automatically adjust to the maximum power output of the input source via the input dynamic power management control (INDPM).

HL7026 manages the complete charging cycle of a Li-ion battery autonomously with or without the presence of an I²C host. It detects the battery voltage and automatically charges the battery in four phases: trickle charge, pre-conditioning, constant current and constant voltage. It automatically terminates charging when the battery is full, and restarts a charging cycle if the battery voltage falls below the recharge threshold. For a short circuit protected battery, it can reactivate the battery by providing a float voltage to the battery terminal before charging starts. Its I²C interface provides maximum programmability for charging parameters and system level communication. When the I²C host is not present, a built in watchdog timer stops charging after the timer expires to assure safety battery operation.

A built in low-resistance power path management system enables instant power-up of the system rail when an input source is plugged in, even with a shorted battery or no battery. When a valid battery is present, it provides battery assistant mode during charging when the system load exceeds the capacity of the input source.

The USB OTG boost function provides a programmable 4.55V~5.51V boost output at VIN port from the battery, and supports current up to 2.1A.

HL7026 integrates comprehensive protections mechanism to ensure safe operation of the battery, including battery temperature monitoring via negative temperature coefficient (NTC) thermistor, charging safety timer, over-voltage and under-voltage detection. The device also provides output over-current protection, and regulates its on-chip junction temperature (T_{J_REG}) to be no more than 120℃ by regulating its charging current.

HL7026 is available in a 24-pin 4mm x 4mm QFN package.

Pin Diagram

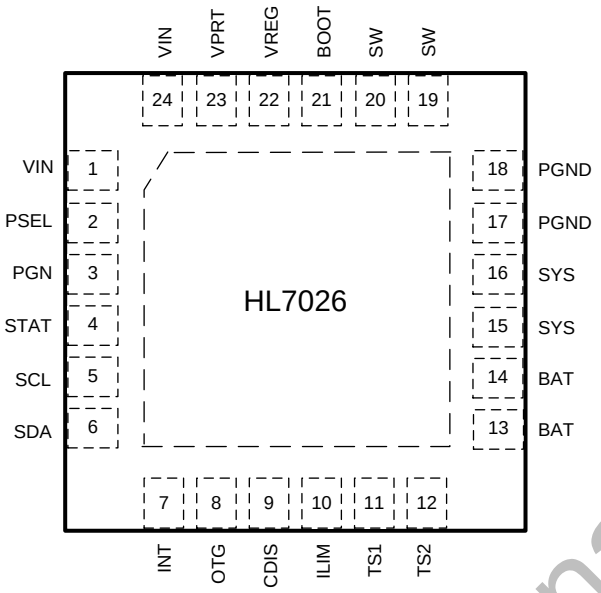


Figure 2 (Top View)

Pin Description

Pin No.	Pin Name	Description
1, 24	VIN	Charger Input Voltage. The internal reverse-block MOSFET (PROTFET) is connected between VIN and VPRT. Place a 1μF ceramic capacitor from VIN to PGND and place it as close as possible to IC.
2	PSEL	Power source selection input. High indicates a USB host source and Low indicates an adapter source.
3	PGN	Open drain active low power good indicator. Connect to the pull up rail via 10kohm resistor. LOW indicates a good input source if the input voltage is between UVLO and V_{VIN_OV}, above SLEEP mode threshold, and current limit is above 30mA.
4	STAT	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10kohm. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks at 1Hz.
5	SCL	I^2C interface serial clock. Connect SCL to 1.8V rail through a 10kΩ pull-up resistor.
6	SDA	I^2C interface serial data. Connect SDA to 1.8V rail through a 10kΩ pull-up resistor.
7	INT	Open-drain Interrupt Output. Connect the INT to a logic rail via 10kΩ resistor. The INT pin sends active low, 256us pulse to host to report charger device status and fault.
8	OTG	USB current limit selection pin during buck mode, and active high enable pin during boost mode. In buck mode with USB host, when OTG = High, I_{IN} LIM = 500mA and when OTG = Low, I_{IN} LIM= 100mA.The boost mode is activated when REG01[5:4]=10 and OTG pin is High.

9	**CDIS**	CDIS Charge Disable Pin. Battery charging is enabled when REG01[5:4]=01 and CDIS pin = Low. CDIS pin must be pulled high or low.
10	**ILIM**	ILIM pin sets the maximum input current limit via an external resistor to PGND. A resistor is connected from ILIM pin to ground to set the maximum limit as $ILIM_{MAX} = (1V/R1) \times K_{ILIM.}$ The actual input current limit is the lower one set by ILIM and by REG00[2:0]. The minimum input current programmed on ILIM pin is 500mA.
11	**TS1**	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from VREG to TS1 to PGND. Charge suspends when TS1 pin is out of range. Recommend 103AT-2 thermistor.
12	**TS2**	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from VREG to TS2 to PGND. Charge suspends when TS2 pin is out of range. Recommend 103AT-2 thermistor.
13, 14	**BAT**	Battery connection point to the positive terminal of the battery pack. The internal PPFET is connected between BAT and SYS. Connect a 10uF capacitor closely to the BAT pin.
15, 16	**SYS**	System connection point. The internal PPFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage.
17, 18	**PGND**	Power ground connection for high-current power converter node. Internally, PGND is connected to the low-side MOSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power ground and the analog ground near the IC PGND pin.
19, 20	**SW**	Switching node connecting to output inductor. Internally SW is connected to the high-side MOSFET (HSFET) and the low-side MOSFET (LSFET). Connect the 100nF bootstrap capacitor from SW to BOOT.
21	**BOOT**	PWM high side driver positive supply. Internally, the BOOT is connected to the anode of the bootstrap diode. Connect the 100nF bootstrap capacitor from SW to BOOT.
22	**VREG**	PWM low side driver positive supply output. Internally, VREG is connected to the anode of the boost-strap diode. Connect a 4.7μF (10V rating) ceramic capacitor from VREG to analog ground. The capacitor should be placed close to the IC. VREG also serves as bias rail of TS1/TS2 pins.
23	**VPRT**	Battery Boost Mode Output Voltage. Connected to the reverse blocking MOSFET (PROTFET) and the high-side MOSFET (HSFET).
-	**Thermal Pad**	There is internal electrical connection between the exposed thermal pad and the ground of the IC. The thermal pad must be connected to the same potential as the GND on the printed circuit board. Do not use the thermal pad as the primary ground input to the device. PGND terminals must be connected to ground at all times.

Table 4 HL7026 Pin Description

Internal Functional Block Diagram

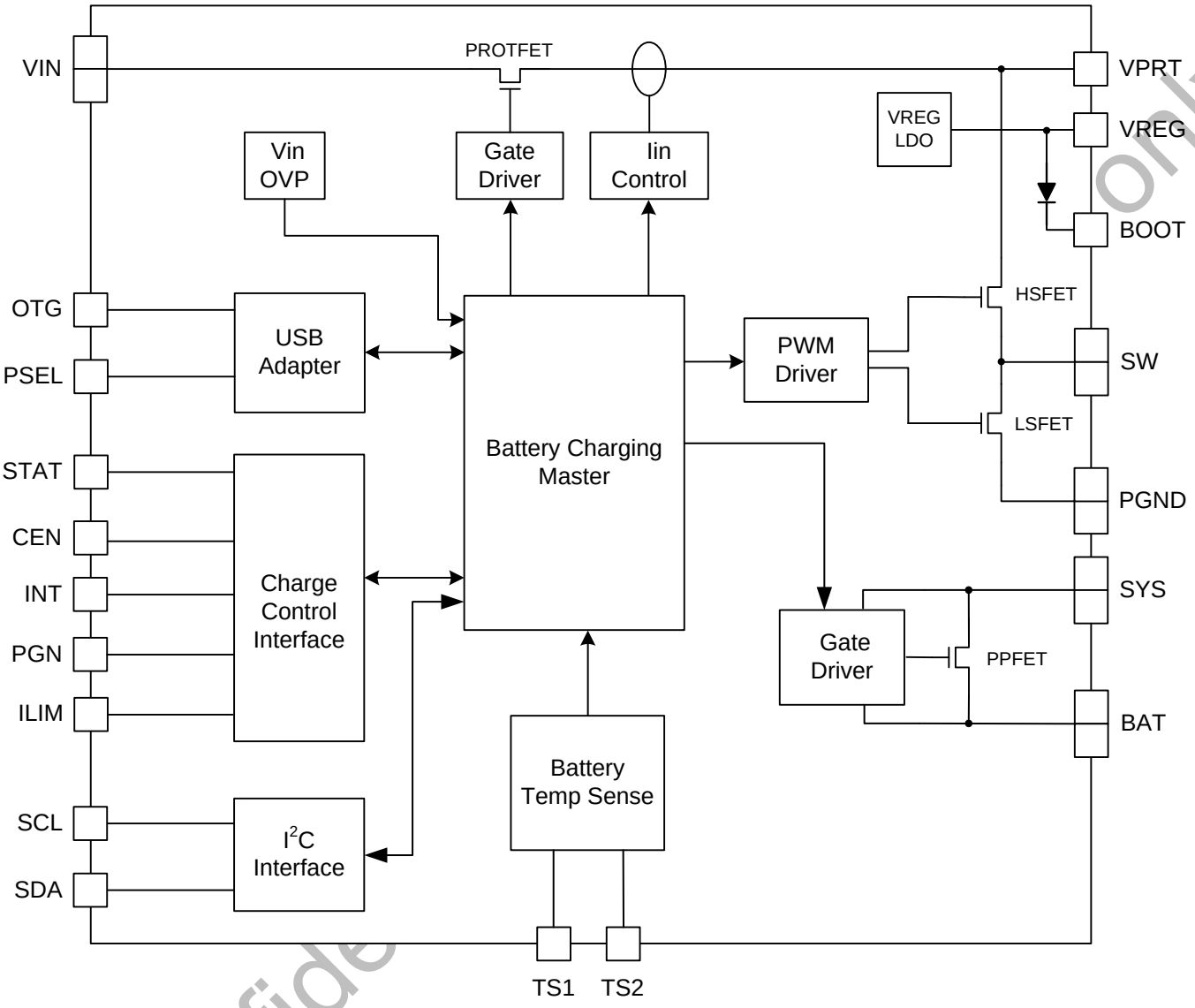


Figure 3 HL7026 Internal Functional Block Diagram

Absolute Maximum Ratings(1)

		VALUE
Voltage range (with respect to GND)	VIN	–1.4 V ~ 20 V
	VPRT	–0.3 V ~ 20 V
	STAT, PGN	–0.3 V ~ 20 V
	BOOT	–0.3 V ~ 20 V
	SW	–0.3 V ~ 20 V
	BAT, SYS (converter not switching)	–0.3 V ~ 5.5 V
	SDA, SCL, INT, OTG, ILIM, VREG, TS1, TS2, CDIS, PSEL	–0.3 V ~ 5.5 V
	BOOT to SW	–0.3 V ~ 5.5 V
	PGND to GND	–0.3 V ~ 0.3 V
Output sink current	INT, STAT, PGN	6mA
Junction-to-ambient thermal resistance	θ_{JA}	34 °C/W
Junction-to-case thermal resistance	θ_{JC}	3 °C/W
Junction temperature	T_J	–40°C to 150°C
Storage temperature	T_{stg}	–65°C to 150°C
Pin soldering temperature	T_s(10s)	260°C
ESD	HBM	1000V
ESD	CDM	250V

Recommended Operating Conditions(2)

		MIN	MAX	UNIT
V_{VIN}	Input voltage	3.9	7	V
I_{VIN}	Input current		3	A
I_{SYS}	Output current (SYS)		4.5	A
V_{BAT}	Battery voltage		4.4	V
I_{BAT}	Fast charging current		4.5	A
	Discharging current with internal MOSFET (PPFET)		6A continuous 9A peak (up to 1 second duration)	A
T_A	Operating free-air temperature range	–40	85	°C

Note

(1) Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40℃ to +85℃ unless otherwise noted.

Electrical Specifications

$V_{VIN\_UVLOZ}<V_{VIN}<V_{OVR}$ & $V_{VIN}>V_{BAT}+V_{SLEEP}$,T_J = -40℃--125℃ and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Currents						
I_{BAT}	Battery discharge current	V_{VIN} < V_{UVLO}, V_{BAT} = 4.2 V, leakage between BAT and VIN			5	uA
		High-Z Mode, or no VIN, PPFET disabled (REG07[5] = 1)		9	20	uA
		High-Z Mode, or no VIN, REG07[5] = 0, –40°C – 85°C		22	55	uA
I_{VIN}	Input supply current(VIN)	V_{VIN} = 5 V, High-Z mode		22	30	uA
		V_{VIN} = 12V, High-Z mode		32		uA
		V_{VIN} > V_{UVLO}, V_{VIN} > V_{BAT}, converter switching, VIN=5V, V_{BAT}=3.8V, I_{SYS}=0A		17		mA
I_{BOOST}	Battery discharge current in boost mode	V_{BAT}=4.2V, Boost mode, I_{VPRT} = 0A, converter switching		7		mA
VIN/BAT Power Up						
V_{VIN_OP}	VIN operating range		3.9		7	V
V_{VIN_UVLO}	VIN for active I^2C, no battery	V_{VIN} rising	3.6	3.9		V
V_{SLEEP}	Sleep mode falling threshold	V_{VIN} falling, $V_{VIN-VBAT}$	14	28	56	mV
V_{SLEEPZ}	Sleep mode rising threshold	V_{VIN} rising, $V_{VIN-VBAT}$	20	39	78	mV
V_{VIN_OV}	VIN over-voltage rising threshold	V_{VIN} rising		7.1		V
$V_{OVR-HYST}$	VIN over-voltage falling Hysteresis	V_{VIN} falling		245		mV
V_{BAT_UVLO}	Battery for active I^2C, no VIN	V_{BAT} rising	2.3			V
V_{BAT_DPL}	Battery depletion threshold	V_{BAT} falling		2.4	2.6	V
$V_{BAT\_DPL\_HY}$	Battery depletion rising hysteresis	V_{BAT} rising		200		mV
V_{VINMIN}	Bad adapter detection threshold	V_{VIN} falling		3.9		V
I_{BADSRC}	Bad adapter detection current source			50		mA
Power Path Management						
V_{SYS_RANGE}	System regulation voltage	Isys = 0A, Q4 off, V_{BAT} up to 4.2 V, REG01[3:1]=101, V_{SYSMIN} = 3.5 V	3.5		4.544	V
V_{SYS_MIN}	System voltage output	REG01[3:1]=101,	3.55	3.65		V

		V_{SYSMIN} = 3.5 V				
$R_{ON\_PROTFET}$	Internal top reverse blocking MOSFET on-resistance	Measured between VIN and VPRT		38		mΩ
R_{ON_HSFET}	Internal high-side switching MOSFET on-resistance between VPRT and SW	T_J = –40°C – 85°C		38		mΩ
		T_J = -40°C – 125°C		38		mΩ
R_{ON_LSFET}	Internal low-side switching MOSFET on-resistance between SW and PGND	T_J = –40°C – 85°C		34		mΩ
		T_J = -40°C – 125°C		34		mΩ
V_{FWD}	PPFET forward voltage in supplement mode	BAT discharge current 10mA		30		mV
V_{SYS_BAT}	SYS/BAT Comparator	V_{SYS} falling		35		mV
V_{BATGD}	Battery good comparator rising threshold	V_{BAT} rising		3.65		V
V_{BATGD_HYST}	Battery good comparator falling threshold	V_{BAT} falling		100		mV
Battery Charger						
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy	V_{BAT} = 4.208V	-0.5		0.5	%
$I_{ICHG\_REG\_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.8V, I_{CHG} = 1792mA, T_J = –20°C – 125°C	–10		10	%
I_{CHG_20pct}	Charge current with 20% option on	V_{BAT} = 2.8V, I_{CHG} = 104mA, REG02=03	75		175	mA
$V_{BATLOWV}$	Battery LOWV falling threshold	Quick charge to pre-charge, REG04[1] = 1	2.6	2.8	2.9	V
$V_{BATLOWV\_HYST}$	Battery LOWV rising threshold	Pre-charge to quick charge, REG04[1] = 1	2.8	3.0	3.1	V
I_{PRECHG_ACC}	Pre-charge current regulation accuracy	V_{BAT} = 2.6V, I_{CHG} = 256mA	–20		20	%
I_{TERM_ACC}	Termination current accuracy	I_{TERM} = 256mA, I_{CHG} = 2048mA	–20		20	%
V_{SHORT}	Battery short voltage	V_{BAT} falling		1.85		V
V_{SHORT_HYST}	Battery short voltage hysteresis	V_{BAT} rising		200		mV
I_{SHORT}	Battery short current	V_{BAT}<2.2V		100		mA
V_{RECHG}	Recharge threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 0		100		mV

t_{RECHG}	Recharge deglitch time	V_{BAT} falling, REG04[0]=0		32		ms
R_{ON_PPFET}	SYS-BAT MOSFET on-resistance	T_J = 25°C		17		mΩ
		T_J = –40°C – 125°C		17		mΩ
Input Voltage/Current Regulation						
$V_{INDPM\_REG\_ACC}$	Input voltage regulation accuracy		–2		2	%
I_{USB_DPM}	USB Input current regulation limit, V_{VIN} = 5V, current pulled from input source	USB100	85	97	100	mA
		USB150	125	142	150	mA
		USB500	440	470	500	mA
		USB900	750		900	mA
I_{ADPT_DPM}	AC adapter regulation accuracy, V_{VIN}=5V	Input current limit 1.5A, REG00[2:0] = 101	1.3	1.46	1.5	A
I_{IN_START}	Input current limit during system start up	V_{SYS}<2.2V		100		mA
K_{ILIM}	I_{IN} = K_{ILIM}/R_{ILIM}	I_{INDPM} = 1.5A	440	485	530	A x Ω
BAT Over-Voltage Protection						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		103		%
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		1		%
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			32		ms
Thermal Regulation and Thermal Shutdown						
T_{J_REG}	Junction temperature regulation accuracy	REG06[1:0] = 11		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		150		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			20		°C
	Thermal shutdown rising deglitch	Temperature increasing delay		1		ms
	Thermal shutdown falling deglitch	Temperature decreasing delay		1		ms
COLD/HOT Thermistor Comparator						
V_{LTF}	Cold temperature threshold in charger mode, TS1/TS2 pin voltage rising threshold	Charger suspends charge. As percentage to V_{VREG}	73	73.5	74	%
V_{LTF_HYS}	Cold temperature hysteresis in charger mode, TS1/TS2 pin voltage falling	As percentage to V_{VREG}		0.06		%
V_{HTF}	Hot temperature in charger	As percentage to V_{VREG}	46.6	47.7	48.8	%

	mode, TS1/TS2 pin voltage falling threshold					
V_{TCO}	Cut-off temperature in charger mode, TS1/TS2 pin voltage falling threshold	As percentage to V_{VREG}	44.2	44.7	45.2	%
	Deglitch time for temperature out of range detection	V_{TS1}& V_{TS2}> V_{LTF}, or V_{TS1}&V_{TS2}< V_{TCO}, or V_{TS1}&V_{TS2}< V_{HTF}		10		ms
V_{LTF_BOOST0}	Cold temperature threshold 0 in boost mode, TS1/TS2 pin voltage rising threshold	As percentage to VREG REG02[1] = 0	75.5	76	76.5	%
$V_{LTF\_HYS\_BOOST0}$	Cold temperature threshold 0 hysteresis in boost mode, TS1/TS2 pin voltage falling threshold	As percentage to VREG REG02[1] = 0 (Approx. 1°C w/ 103AT)		1		%
V_{LTF_BOOST1}	Cold temperature threshold 1 in boost mode, TS1/TS2 pin voltage rising threshold	As percentage to VREG REG02[1] = 1 (Approx. -20°C w/ 103AT)	78.5	79	79.5	%
$V_{LTF\_HYS\_BOOST1}$	Cold temperature threshold 1 hysteresis in boost mode, TS1/TS2 pin voltage falling threshold	As percentage to VREG REG02[1] = 1 (Approx. 1°C w/ 103AT)		0.43		%
V_{HTF_BOOST0}	Hot temperature threshold 0 in boost mode, TS1/TS2 pin voltage falling threshold	As percentage to VREG REG06[3:2] = 01 (Approx. 55°C w/ 103AT)		36		%
V_{HTF_BOOST1}	Hot temperature threshold 1 in boost mode, TS1/TS2 pin voltage falling threshold	As percentage to VREG REG06[3:2] = 00 (Approx. 60°C w/ 103AT)		33		%
V_{HTF_BOOST2}	Hot temperature threshold 2 in boost mode, TS1/TS2 pin voltage falling threshold	As percentage to VREG REG06[3:2] = 10 (Approx. 65°C w/ 103AT)		30		%
Charge Over-Current Comparator						
I_{HSFET_OCP}	HSFET over-current threshold		5.3	7.5		A
I_{PPFET_OCP}	System over load threshold		5.5	9.0		A
F_{SW}	PWM switching frequency, and digital clock		1300	1500	1700	kHz
D_{MAX}	Maximum PWM duty cycle			99		%
BOOST Mode Operation						

V_{OTG_REG}	OTG output voltage	I_{VIN}=0 , REG06[7:4] = 0111 (4.998 V)		5		V
$V_{OTG\_REG\_ACC}$	OTG output voltage accuracy	I_{VIN}=0 , REG06[7:4] = 0111 (4.998 V)	-3		3	%
V_{OTG_BAT}	Battery voltage exiting OTG mode	BAT falling, REG04[1] = 1	2.9			V
I_{OTG}	OTG mode output current	REG01[0]=0	1			A
		REG01[0]=1	2.1			A
V_{OTG_OVP}	OTG over voltage threshold	VIN rising	5.9	6.1	6.3	V
$V_{OTG\_OVP\_HYS}$	OTG over-voltage threshold hysteresis	VIN falling		200		mV
V_{OTG_LSZOCP}	LSFET cycle-by-cycle current limit			6.4		A
VREG LDO						
V_{VREG}	VREG LDO output voltage	V_{VIN}=6V，I_{VREG}=40mA	4.75	5.0	5.25	V
		V_{VIN}=5V，I_{VREG}=20mA	4.5	4.77		V
I_{VREG}	VREG LDO current limit	V_{VIN}=5V，V_{VREG}=3.8V		76		mA
Logic I/O Pin Characteristics(OTG,CDIS,PSEL,PGN)						
V_{IL}	Input low threshold (OTG, CDIS)				0.4	V
V_{IH}	Input high threshold (OTG, CDIS)		1.05			V
V_{OL}	STAT output low saturation voltage	Sink current = 5 mA			0.4	V
I_{BIAS}	High level leakage current (OTG, CDIS)	Pull up rail 1.8V			1	uA
I_{LKG_STAT}	STAT leakage current	STAT in high impedance, and STAT=20V			1	uA
I^2C Interface (SDA, SCL, INT)						
V_{IH}	Input high threshold level	$V_{PULL-UP}$ = 1.8V, SDA and SCL	1.05			V
V_{IL}	Input low threshold level	$V_{PULL-UP}$ = 1.8V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{BIAS}	High-level leakage current	$V_{PULL-UP}$ = 1.8V, SDA and SCL			1	uA
I_{LKG_INT}	INT leakage current	INT in high impedance, and INT=5V			1	uA
f_{SCL}	SCL clock frequency				400	kHz
Digital Clock And Watchdog Timer						
f_{HIZ}	Digital crude clock	VREG LDO disabled	100	125	150	kHz
f_{DIG}	Digital clock	VREG LDO enabled	1350	1500	1650	kHz

Table 5 Electrical Specifications

Typical Characteristics

$V_{VIN\_UVLOZ}<V_{VIN}<V_{OVR}$ & $V_{VIN}>V_{BAT}+V_{SLEEP}$,T_J = -40℃--125℃ and T_J = 25°C for typical values unless other noted.

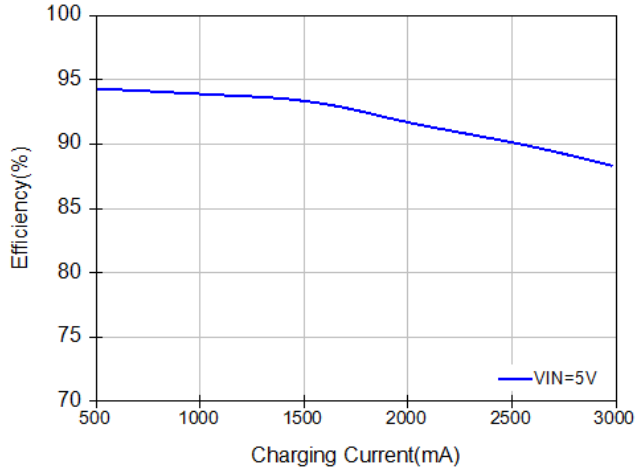


Figure 4 Charging Efficiency vs. Charging Current

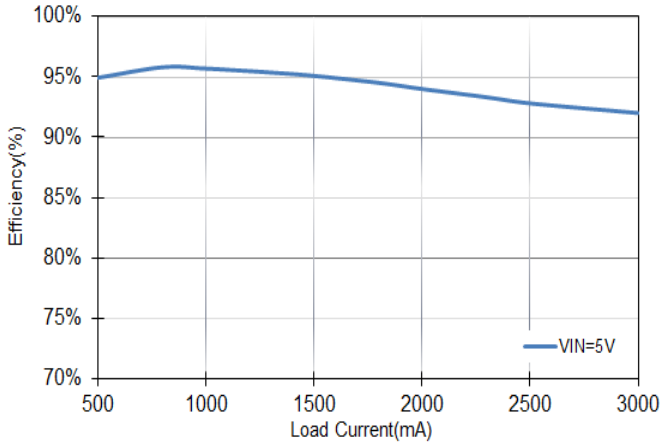


Figure 5 System Efficiency vs. System Load Current

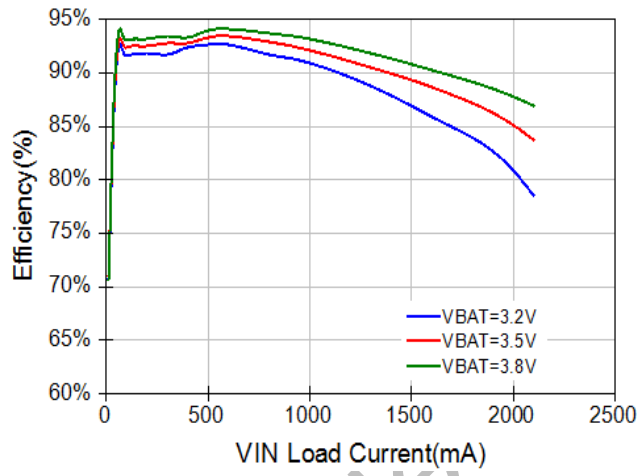


Figure 6 Boost Mode Efficiency vs. VIN Load Current

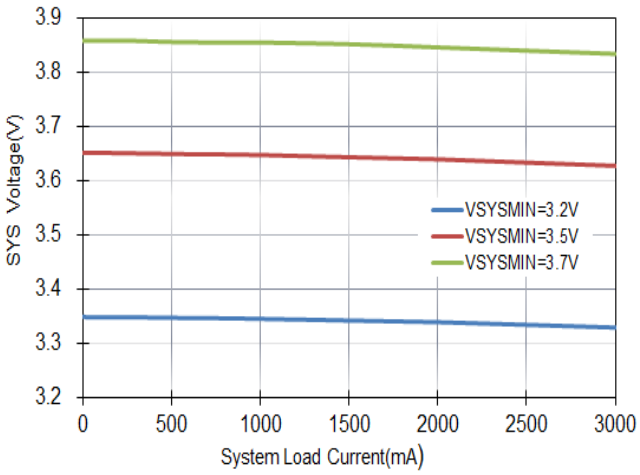


Figure 7 SYS Voltage Regulation vs. System Load Current

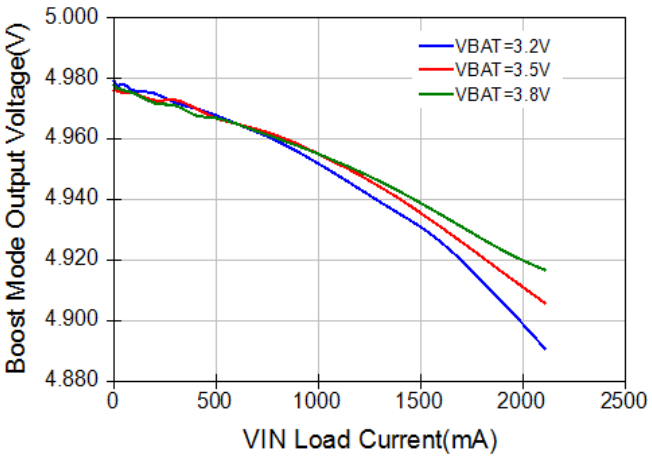


Figure 8 Boost Mode VIN Voltage Regulation vs. VIN Load Current

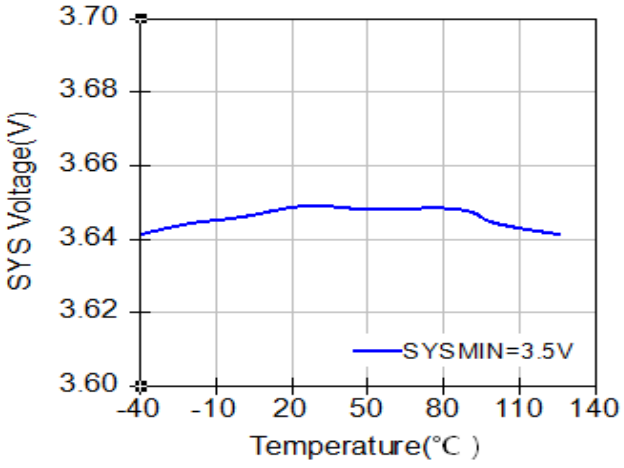


Figure 9 SYS Voltage vs. Temperature

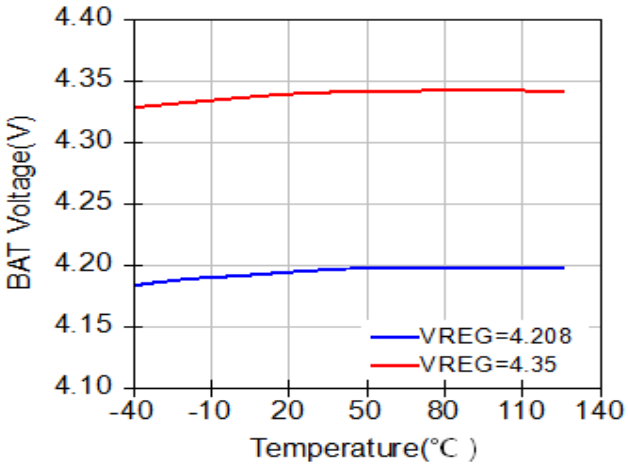


Figure 10 BAT Voltage vs. Temperature

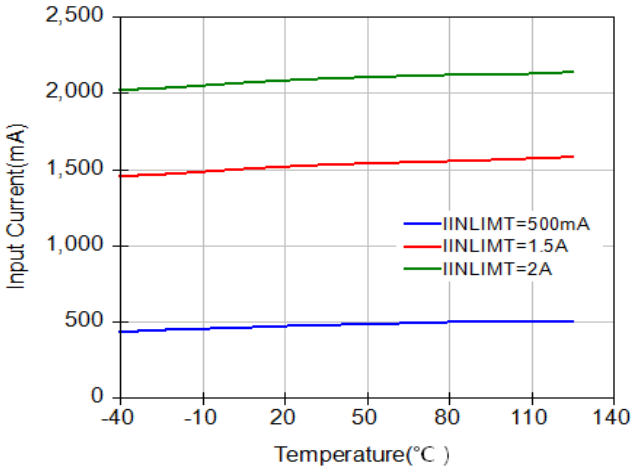


Figure 11 Input Current Limit vs. Temperature

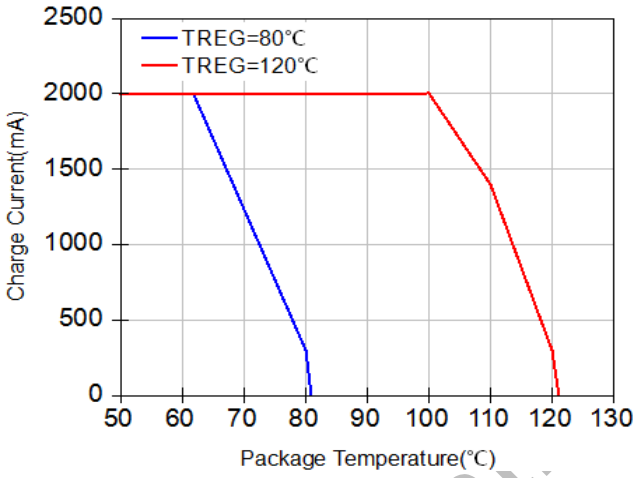


Figure 12 Charge Current vs. Package Temperature

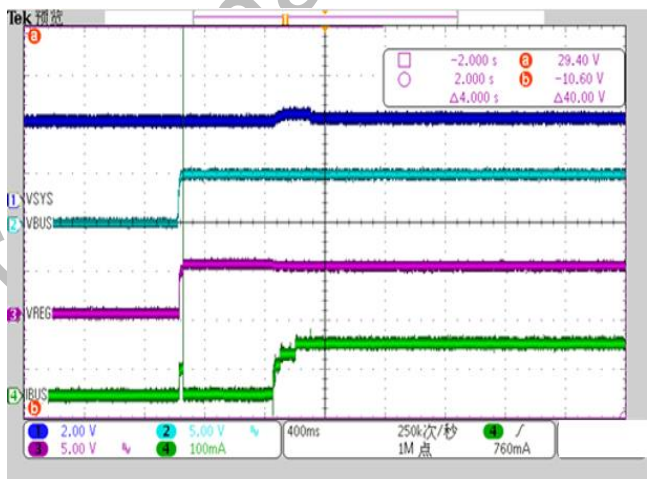


Figure 13 Power Up with Charge Enabled(V_{BAT}=3.2V)

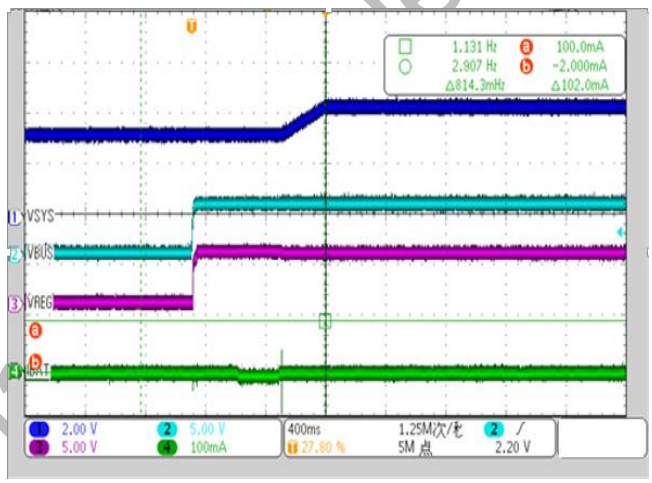


Figure 14 Power Up with Charge Disabled(V_{BAT}=3.2V)

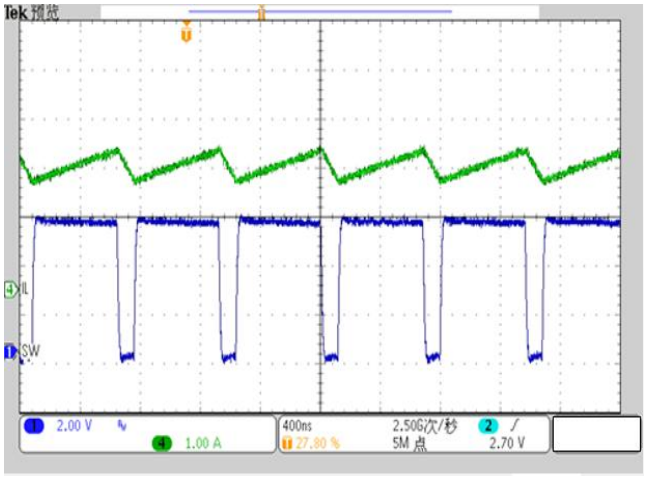


Figure 15 PWM Switching in Buck Mode

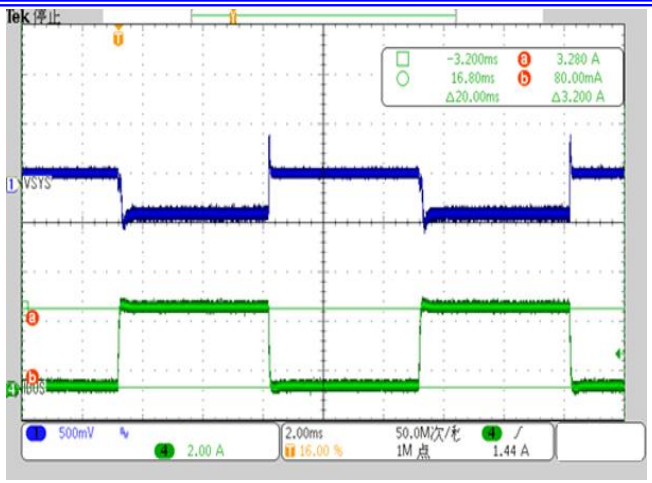


Figure 16 Input Current DPM Response Without Battery

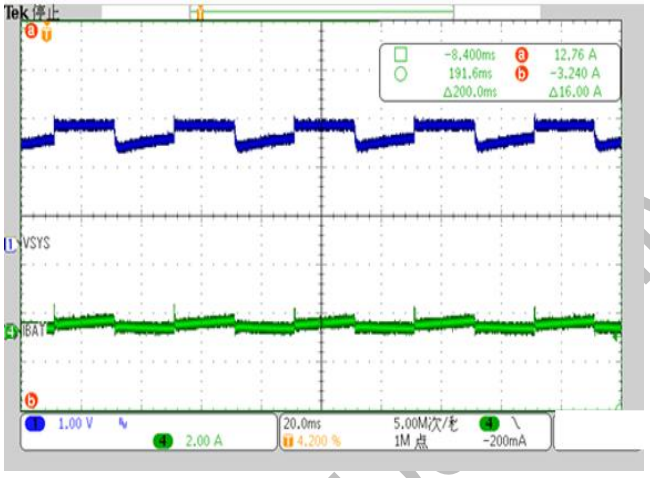


Figure 17 Load Transient During Supplement Mode

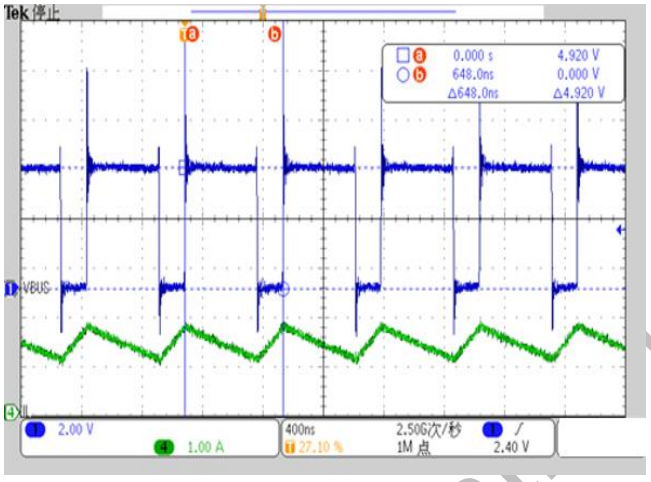


Figure 18 Boost Mode Switching

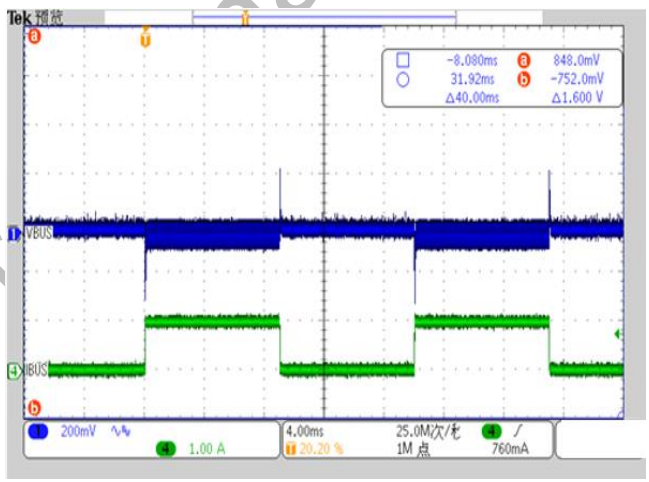


Figure 19 Boost Mode Load Transient

Detailed Description

The HL7026 is a single cell Li-ion battery charger with power path management and I²C interface. The device integrates the input reverse blocking MOSFET (PROTFET), high-side switching MOSFET (HSFET), low-side switching MOSFET (LSFET), and power-path MOSFET (PPFET) between system and battery. The device also integrates the bootstrap diode for the high-side gate driver.

Device Power Up

Power-On-Reset (POR)

The internal circuits are powered from the higher voltage of VIN and V_{BAT}. When VIN or V_{BAT} rises above V_{BAT_UVLO}, the battery depletion comparator and PPFET driver are active. I²C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Power Up from Battery

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPL}), the PPFET turns on and connects battery to system. The Low-Drop-Out (LDO) regulator on VREG pin stays off to minimize the quiescent current. The low R_{DSON} in PPFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through PPFET. When the system is overloaded or shorted, the device will immediately turn off PPFET and keep PPFET off until the input source plugs in again.

Turn Off Power Path

The PPFET can be turned off by the I²C host through REG07[5]. This bit allows the user to independently turn off the PPFET when the battery condition becomes abnormal during charging. When PPFET is off, there is no path to charge or discharge the battery.

When battery is not attached, the PPFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.

Shipping Mode

When end equipment is assembled, the system is connected to battery through PPFET. There will be a small leakage current to discharge the battery even when the system is powered off. In order to extend the battery life during shipping and storage, the device can turn off PPFET so that the system voltage is zero to minimize the leakage.

In order to keep PPFET off during shipping m01ode, the host has to disable the watchdog timer (REG05[5:4]=00) and disable PPFET (REG07[5]=1) at the same time.

Power Up from External DC Source

When the DC source plugs in, the HL7026 checks the input source voltage to turn on VREG LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

VREG LDO

The VREG LDO supplies internal circuits as well as the power HSFET & LSFET gate drivers. The LDO also provides a bias rail to external resistors connected to TS1/TS2 pin. The pull-up rail of STAT can be connected to VREG as well.

The VREG is enabled when all the conditions valid:

1. V_{VIN} is higher than V_{VIN_UVLO}.
2. V_{VIN} is higher than V_{BAT} + V_{SLEEPZ} in buck mode, or V_{VIN} is lower than V_{BAT} + V_{SLEEPZ} in boost mode.
3. After typical 220ms delay (100 ms minimum) is complete.

If one of the above conditions is not valid, the device is in high impedance mode with REGN LDO off. The device

draws less than I_{VIN} (15 µA typical) from VIN during high impedance state. The battery powers up the system when the device is in high impedance mode.

Input Source Qualification

After VREG LDO powers up, HL7026 checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VIN voltage below V_{VIN_OV} (7.1V typical).
2. VIN voltage above V_{VIN_UVO} (3.9V typical) when pulling 30mA (poor source detection).

Once the input source passes all the above conditions, the status register REG08[2] goes high and PGN goes low. An INT assertion pulse is sent. If the device fails the above validation conditions, it will repeat the detection every 2 seconds.

Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 3A.

After REG08[2] goes HIGH or PGN is low, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in high impedance mode during host mode.

The HL7026 sets input current limit through PSEL and OTG pins according to Table 6. After the input current limit detection is done, the input source type is listed in REG08[7:6], and input current limit value updated in REG00[2:0]. The host can also write to REG00[2:0] to change the input current limit.

PSEL/OTG Pin Setting

HL7026 directly takes the external USB PHY device output to decide whether the input is USB host or charging port.

PSEL	OTG	INPUT CURRENT LIMIT	REG08[7:6]
HIGH	LOW	100 mA	01
HIGH	HIGH	500 mA	01
LOW	—	3A	10

Table 6 Input Current Limit Detection

High Impedance State with 100mA USB Host

In battery charging specification, the good battery threshold is the minimum charge level of a battery to power up the portable device successfully. When the input source is 100mA USB host, and the battery is above good-battery threshold (V_{BATGD}, 3.65V typical), the device follows battery charging spec and enters high impedance state. In this state, the device is in the lowest quiescent state with VREG LDO and most internal circuits and power devices turned off. To enter high impedance mode, the device sets REG00[7] to 1.

Once the device enters high impedance state in host mode, it stays in high impedance until the I^2C host writes REG00[7]=0. When the host wakes up, it is recommended to first check if the device is in high impedance state.

In default mode, the device will reset REG00[7] back to 0 when input source is removed. When another source plugs in, the charger IC will run detection again, and update the input current limit.

Forced Input Current Limit Detection

When adapter is plugged-in, the host can force the

charger device to run input current limit detection by setting REG07[7]=1. After the detection is complete, REG07[7] will return to 0 by itself. And new input current limit is set based on PSEL/OTG .

Buck PWM Converter Power-Up

After the input current limit is set, the buck converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, PPFET turns off. Otherwise, PPFET stays on to charge the battery.

The HL7026 provides soft-start when ramping up the system rail SYS by limiting the peak inductor current. The charger device sets the input current limit to be the lower value between register setting and ILIM pin.

As a battery charger, the HL7026 work as a fixed frequency 1.5MHz step-down switching regulator. The fixed frequency operation keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature. All loop compensation components are internal, and the topology is chosen so that low ESR ceramic capacitors can be used for the output LC filter.

PWM Converter in Boost Mode Operation

The HL7026 supports boost converter operation to deliver power from the battery to other portable devices through VIN or VPRT port. The boost mode output provides a maximum output current of 2.1A. The boost operation can be enabled if the following conditions are valid:

1. V_{BAT} above V_{OTG_BAT} threshold (set by REG04[1]).
2. V_{VIN} less than V_{BAT} + V_{SLEEP} (in sleep mode).
3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4]=10).
4. After 30ms delay from boost mode enable.
5. Thermistor Temperature is within boost mode temperature monitor threshold unless BHOT[1:0] is set to 11(REG06[1:0]) to disable this monitor function.

In boost mode, the HL7026 is configured as a 1.5MHz step-up switching regulator. A proprietary control scheme is used to optimize VIN load transient performance. The device switches from PWM operation to PFM operation at light load to improve efficiency.

During boost mode, the status register REG08[7:6] is set to 11, and the output current can reach up to 2.1 A, selected via I^2C (REG01[0]). The boosted output voltage can be programmed from 4.55 V to 5.5 V by changing BOOSTV bits (REG06[7:4]).

Any fault during boost operation, including VIN over-voltage or over-current, sets the fault register REG09[6] to1 and an INT is asserted.

Power Path Management

The HL7026 accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VIN), battery (BAT), or both.

The device separates system from battery with PPFET. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5V).

When the battery is below minimum system voltage setting, the PPFET operates in linear charging mode, and the system rail SYS is always regulated to be 150mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, PPFET is fully turned on and the voltage difference between the system and battery is the V_{DS} of PPFET.

When the battery charging is disabled or terminated, the system is also regulated at 150mV above the minimum system voltage setting or V_{BAT}+80mV, whichever is higher. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

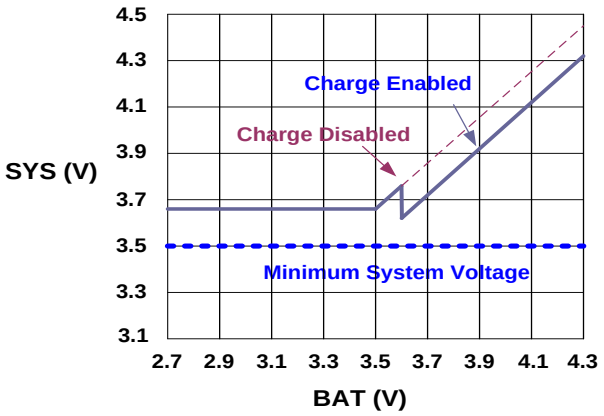


Figure 20 SYS voltage vs. BAT voltage with Power Path

Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, HL7026 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters battery assist mode where the PPFET turns on and battery starts discharging so that the system is supported from both the input source and battery. During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

Figure 21 shows the DPM response with 5V/1.2A adapter, 3.2V battery, 2.0A charge current and 3.4V minimum system voltage setting.

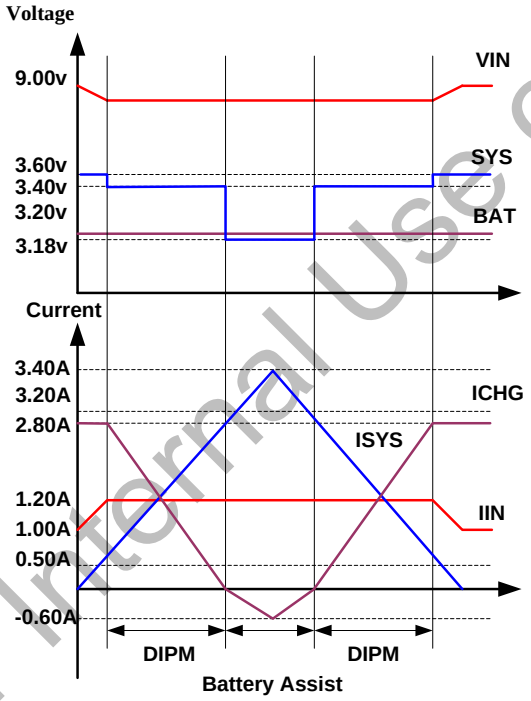


Figure 21 DPM response

Supplement Mode

When the system voltage falls below the battery voltage by more than 30mV, the PPFET turns on to support any additional current SYS may need that the buck converter cannot support. When the system load becomes light again that SYS becomes slightly higher than BAT, PPFET turns off, and system load is entirely supported by buck regulator.

Figure 22 shows the V-I curve of the PPFET gate regulation operation. PPFET turns off to exit supplement mode when the battery is below battery depletion threshold.

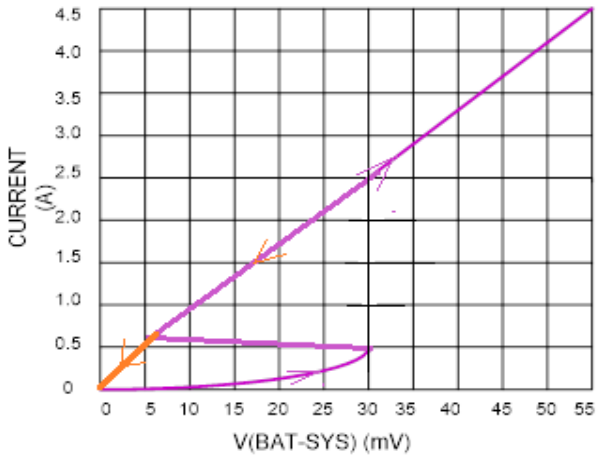


Figure 22 PPFET V-I Curve

Battery Charging Management

The HL7026 charges 1-cell Li-Ion battery with up to 3A charge current. The 17mΩ PPFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), the HL7026 can complete a charging cycle without host involvement. The device default charging parameters are listed in Table7.

DEFAULT MODE	HL7026
Charging Voltage	4.208 V
Charging Current	2.048 A
Pre-charge Current	256 mA
Termination Current	256 mA
Temperature Profile	Hot/Cold ;
Safety Timer	8 hours (see Charging Safety Timer section)

Table 7 Charging Parameter Default Setting

A new charge cycle starts when all the following conditions are valid:

1. Converter starts.
2. Battery charging is enabled by REG01[5:4]= 01 and CDIS pin is low.
3. No thermistor fault on TS1/TS2 pin.
4. No safety timer fault.
5. PPFET is not forced to turn off (REG07[5]=0).

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), HL7026 automatically starts another charging cycle. After the charge done, either toggle CDIS pin or REG01[5:4] will initiate a new charging cycle.

The STAT output indicates the charging status of charging (Low), charging complete or charge disable (High) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies appropriate charging current.

V_{BAT}	CHARGING CURRENT	REG DEFAULT SETTING	REG08[5:4]
$V_{BAT} < V_{SHORT}$ (2V typical)	100mA	–	01

$V_{SHORT} \leqslant V_{BAT} < V_{BATLOWV}$(Typical 2V $\leqslant V_{BAT} <$ 3V)	REG03[7:4]	256mA	01
$V_{BAT} \geqslant V_{BATLOWV}$ (Typical $V_{BAT} \geqslant$ 3V)	REG02[7:2]	2048mA	10

Table 8 Charging Current Setting

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half of the clock rate.

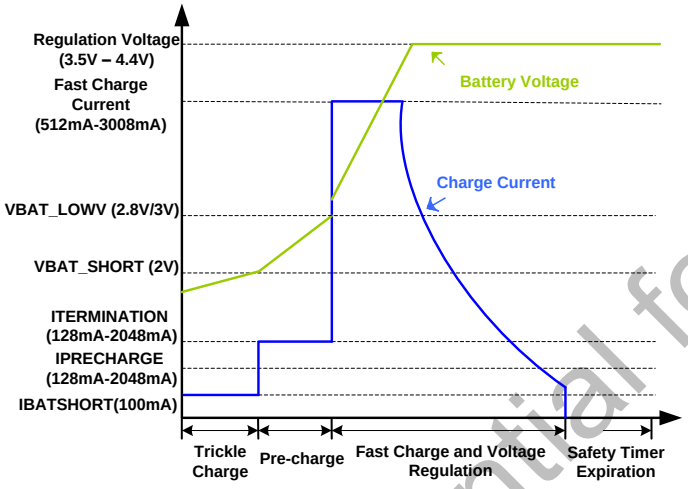


Figure 23 Battery Charging Phases

Monitor Cold/Hot Temperature

The HL7026 continuously monitors battery temperature by measuring the voltage between the TS1/TS2 pin and ground, typically determined by a negative temperature coefficient (NTC) thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds, else the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.

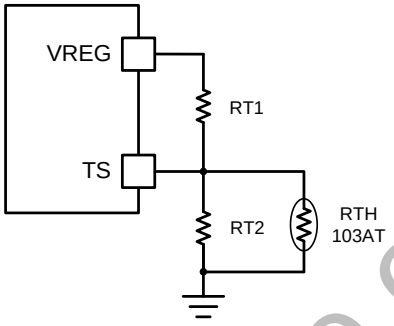


Figure 24 TS1/TS2 Resistor Network

When the TS1/TS2 fault occurs, the fault register REG09[2:0] indicates the actual condition on TS1/TS2 pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

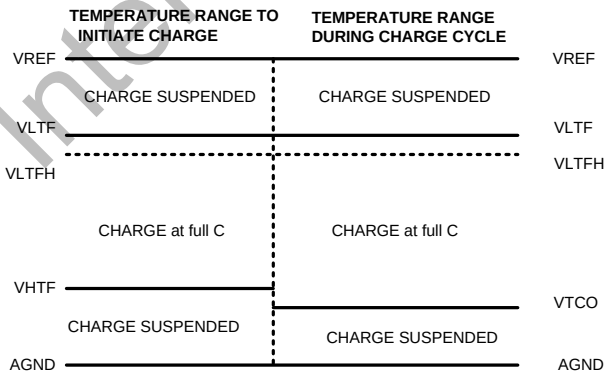


Figure 25 TS1/TS2 Pin Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor is used on the battery pack, the value RT1 and RT2 can be determined by using the following equation:

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (1)$$

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times (\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}})}{RTH_{HOT} \times (\frac{V_{VREF}}{V_{TCO}} - 1) - RTH_{COLD} \times (\frac{V_{VREF}}{V_{LTF}} - 1)}$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery, RTH_{COLD} = 27.28 kΩ

RTH_{HOT} = 4.911 kΩ

RT1 = 5.52 kΩ

RT2 = 31.23 kΩ

Charging Termination

The HL7026 terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the PPFET turns off. The converter keeps running to power the system, and PPFET can turn back on to engage supplement mode. When termination occurs, the status register REG08[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].

Termination when REG02[0] = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through CDIS pin or REG01[5:4].

Charging Safety Timer

The HL7026 has safety timer to prevent extended charging cycle due to abnormal battery conditions.

Te safety timer is 4 hours when the battery is below $V_{BATLOWV}$ threshold. The user can program fast charge safety timer through by REG05[2:1]. When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via REG05[3].

The following actions restart the safety timer after safety timer expires:

•Toggle the CDIS pin High to Low to High (charge enable)

• Write REG01[5:4] from 00 to 01 (charge enable)

• Write REG05[3] from 0 to 1 (safety timer enable)

During input voltage/current regulation or thermal regulation, the safety timer counts at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

USB Timer When Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45min max timer. At the end of the timer, the device stops the converter and goes to high impedance mode.

Status Outputs (PGN, STAT and INT)

Power Good Indicator (PGN)

In HL7026, PGN goes Low to indicate a good input source when:

1. V_{VIN} above V_{VIN_UVLO}
2. V_{VIN} above battery (not in sleep)
3. V_{VIN} below VACOV threshold
4. above V_{VIN_MIN} when I_{BADSRC} current is applied (not a poor source)

Charging Status Indicator (STAT)

The HL7026 indicates charging state on the open drain STAT pin. The STAT pin can drive an LED to visually indicate charging status according to Table9.

CHARGING STATE	STAT

Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS1 /TS2 fault, timer fault, input or system over-voltage)	blinking at 1Hz

Table 9 STAT Pin State

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system about the device operation. Any of the following events will generate a 256us wide active-low pulse on INT pin, referred to as an INT assertion.

• USB/adapter source identified (through DIPM detection)
• Good input source detected
• Input removed or above V_{VIN_OV}
• Charge Complete
• Any fault event in REG09

When a fault occurs, the charger device sends out an INT pulse and latches the fault state in REG09 until the host reads the fault register. The NTC fault is not latched and always reports the current thermistor conditions.

Protections

Input Current Limit Setting on ILIM

For safer operation, the HL7026 also uses ILIM pin to place a hardware limit on the maximum allowed input current. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times 530 \quad (2)$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and ILIM has a 353Ω resistor to ground for 1.5A, the actual input current limit will be set to 1.5A. ILIM pin can be used to set the input current limit rather than the register settings.

The device detects ILIM pin at 1 V. If ILIM voltage exceeds 1 V, the device enters input current regulation. The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current as following:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (3)$$

Thermal Regulation and Shutdown

The HL7026 monitors the internal device junction temperature T_J to avoid overheating the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device reduces the charge current until junction temperature maintains at or below the preset limit. The wide thermal regulation limit range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter if junction temperature reaches the shutdown limit for any reason. The fault register

REG09[5:4] is 10 and an INT is asserted to the host.

During boost mode, the thermal shut-down protection is also enabled and behaves similarly to when the device is in buck and charge mode. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

Buck Mode Protection

The HL7026 closely monitors the input and system voltage, as well as HSFET and LSFET current for safe buck mode operation.

Input Over Voltage Protection

The maximum input voltage for buck mode operation is set at V_{VIN_OVP}. If VIN voltage exceeds this limit, the device stops switching immediately to protect internal circuitry. The fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

System Over Voltage Protection

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

Boost Mode Protection

Output Over Current

The device monitors peak inductor current during boost operation. When it reaches over-current threshold I_{LSFET_OCP}, LSFET is turned off, and HSFET turned on for enough time for the inductor current to discharge before LSFET is allowed to turn on again. If 16 consecutive such events happen, the PWM converter is immediately turned off for around 20ms, and the PWM controller attempts to start up again. REG09[6] is set and an INT is asserted to the host.

If the boost output voltage becomes lower than V_{BAT} due to any reason, the PWM converter is turned off immediately for around 20ms, and the PWM controller attempts to start up again. REG09[6] is set and an INT is asserted to the host.

Output Over Voltage

The maximum output voltage for buck mode operation is set at V_{OTG_OVP}. If VIN voltage exceeds this limit, the device stops switching immediately to protect internal circuitry. The fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

Battery Protection

Battery Over-Voltage Protection

The battery over-voltage limit is clamped at V_{BAT_OVP} (4% nominal) above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[3] goes high and an INT is asserted to the host.

Battery Short Protection

If the battery voltage falls below V_{SHORT} (2V typical), the device immediately turns off PPFET to disable the battery charging or supplement mode. 1ms later, the PPFET turns on and charge the battery with 100-mA current. The device does not turn on PPFET to discharge a battery that is below 2.5 V.

System Over-Current Protection

If the system is shorted or exceeds the over-current limit, the device latches off PPFET. DC source insertion on VBUS is required to reset the latch-off condition and turn on PPFET.

Serial Interface Description

I²C is a 2 wire serial interface developed by Philips Semiconductor (see I²C Bus Specification, version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with a pull-up device. When the bus is idle, both SDA and SCL lines are pulled high. All I²C compatible devices connect to the I²C SDA and SCL buses through open drain I/O pins. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific condition that indicates the START and STOP of data transfer. A slave device receives and /or transmits data on the bus under control of the master device.

HL7026 works as a slave and is compatible with the following data transfer modes as defined in the I²C Bus Specification: Standard mode (100kbps), Fast mode (400kbps), Fast mode plus (1000kbps) and High-speed mode (up to 3.4Mbps in write mode). The interface adds flexibility to the device by making most functions and parameters programmable through the I²C host.

The data transfer protocol for Standard mode, Fast mode and Fast mode plus is the same, therefore referred to as F/S mode in this document. The protocol for High-speed mode is different and referred to as HS mode. The HL7026 device has an initial 7b I²C address of 1101011 (6BH).

F/S Mode Protocol

The master initiates data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high. The master stops data transfer by generating a STOP condition, in which a low-to-high transition occurs on the SDA line while SCL is high. This is shown in Figure 26.

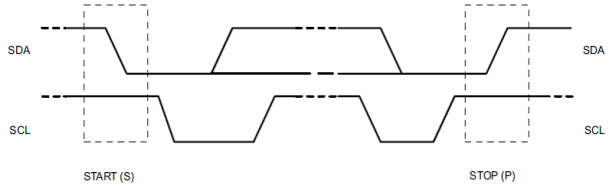


Figure 26 START and STOP Condition

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 27)

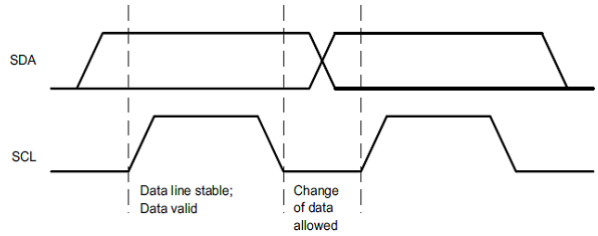


Figure 27 Bit Transfer on the Serial Interface

All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates a acknowledge (see Figure 28) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

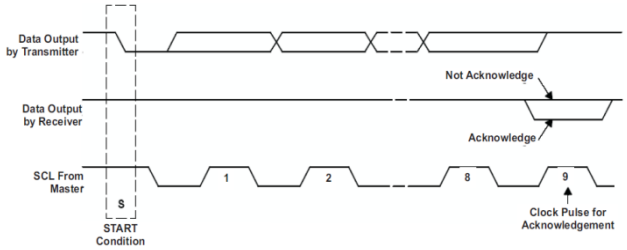


Figure 28 Acknowledge on the I²C Bus

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high(see Figure 29). This releases the bus and stops the communication link with the addressed slave.

All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address. If a transmission is terminated in advance, the master needs to send a STOP condition to prevent the slave I²C logic from getting stuck in a bad state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

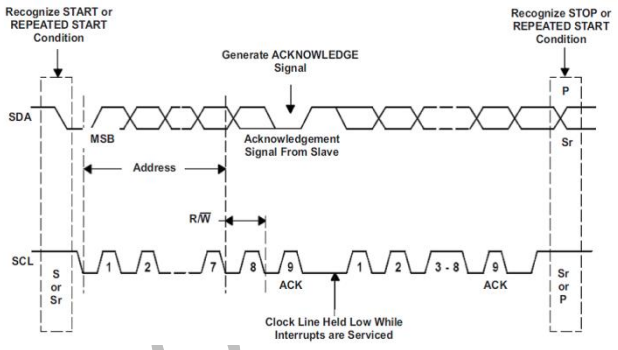


Figure 29 Bus Protocol

I²C Update Sequence

The IC requires a START condition, a valid I²C address, a register address byte, and a data byte for a single update. After receiving of each byte, the IC sends acknowledge by pulling the SDA line low during the high period of a single clock. A valid I²C address will selects this IC. The IC performs an update on the falling edge of the acknowledge signal that follows the LSB bit.

For the first update, the IC requires a START condition, a valid I²C address, a register address byte and a data byte. For all consecutive updates, the IC needs a register address byte and a data byte. Once a STOP condition is received, the IC releases the I²C bus and waits for a new START condition.

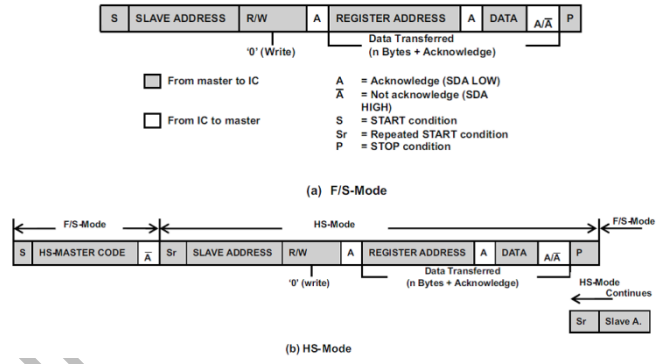


Figure 30 Data Transfer Format in F/S mode and H/S mode

Slave Address Byte

MSB							LSB
1	1	0	1	0	1	1	X

The slave address byte is the first byte received following the START condition from the master device.

Register Description

Slave address: 6BH. REG00-07 support Read and Write. REG08-0A are read only.

Register		Address							
Name	**Hex Address**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Input Control	00H	0	0	0	0	0	0	0	0
Power-On Configuration	01H	0	0	0	0	0	0	0	1
ICharge Control	02H	0	0	0	0	0	0	1	0
PC/TC Control	03H	0	0	0	0	0	0	1	1
VCharge Control	04H	0	0	0	0	0	1	0	0
Charge Termination/Timer Control	05H	0	0	0	0	0	1	0	1
Boost Voltage/Thermal Regulation	06H	0	0	0	0	0	1	1	0
Operation Control	07H	0	0	0	0	0	1	1	1
System Status	08H	0	0	0	0	1	0	0	0
Fault Register	09H	0	0	0	0	1	0	0	1
Vender Info	0AH	0	0	0	0	1	0	1	0
Shipping Mode	0BH	0	0	0	0	1	0	1	1
IR Compensation/Boost Control	0CH	0	0	0	0	1	1	0	0
Misc Operation Control	0DH	0	0	0	0	1	1	0	1

Table 10 Register Description

Bit Definitions

The following table defines the operation of each register bit. Bold font indicates power-on default values.

Bit	Name	Value	Type	Function	
Input Control Register REG00, Address: 00 (Default Value: 00110000, or 30)					
7	EN_HIZ	**0**	R/W	**Disable**	
		1		Enable	
6:3	VINDPM	0000	R/W	3.88V	REG0D[5]=0
		0001		3.96V	
		0010		4.04V	
		0011		4.12V	
		0100		4.20V	
		0101		4.28V	
		0110		**4.36V**	
		0111		4.44V	
		1000		4.52V	
		1001		4.60V	
		1010		4.68V	
		1011		4.76V	
		1100		4.84V	
		1101		4.92V	
		1110		5.00V	
		1111		5.08V	
		0000	R/W	8.32V	REG0D[5]=1
		0001		8.50V	
		0010		8.64V	
		0011		8.82V	
		0100		9.01V	
		0101		9.19V	
		0110		9.33V	
		0111		9.51V	
		1000		9.69V	
		1001		9.87V	
		1010		10.01V	
		1011		10.19V	
		1100		10.38V	
		1101		10.56V	

		1110		10.70V	
		1111		10.88V	
2:0	IINLIM	**000**	R/W	**100mA**	Input current limit, actual input current limit is the lower of I²C and ILIM Pin. Note: PSEL = Lo : 3 A (111) PSEL = Hi : 100 mA (000) (OTG pin = Lo) or 500 mA (OTG pin = Hi)
		001		150mA	
		010		500mA	
		011		900mA	
		100		1A	
		101		1.5A	
		110		2A	
		111		3A	
Power-On Configuration Register REG01, Address: 01 (Default Value: 00011011, or 1B)					
7	Register Reset	**0**	R/W	**Keep current register setting**	
		1		Reset to default. Back to 0 after register reset.	
6	I²C Watchdog Timer Reset	**0**	R/W	**Normal**	
		1		Reset. Back to 0 after register reset.	
5:4	CHG_CONFIG	00	R/W	Charge Disable	
		01		**Charge Battery**	
		10		OTG	
		11			
3:1	SYS_MIN	000	R/W	3.0V	Minimum system voltage limit
		001		3.1V	
		010		3.2V	
		011		3.3V	
		100		3.4V	
		101		**3.5V**	
		110		3.6V	
		111		3.7V	
0	BOOST_LIM	0	R/W	1A	Boost Mode Current Limit
		1		**2.1A**	

ICharge Control Register REG02, Address: 02 (Default Value: 01100000, or 60)

7:2	ICHG		R/W	Binary	(mA)		Binary	(mA)		Binary	(mA)
				0000 00	512		0100 00	1536		1000 00	2560
				0000 01	576		0100 01	1600		1000 01	2624
				0000 10	640		0100 10	1664		1000 10	2688
				0000 11	704		0100 11	1728		1000 11	2752

				0001 00	768		0101 00	1792		1001 00	2816
				0001 01	832		0101 01	1856		1001 01	2880
				0001 10	896		0101 10	1920		1001 10	2944
				0001 11	960		0101 11	1984		1001 11	3008
				0010 00	1024		**0110 00**	**2048**		Note: ICHG higher than 3008mA is not supported.	
				0010 01	1088		0110 01	2112			
				0010 10	1152		0110 10	2176			
				0010 11	1216		0110 11	2240			
				0011 00	1280		0111 00	2304			
				0011 01	1344		0111 01	2368			
				0011 10	1408		0111 10	2432			
				0011 11	1472		0111 11	2496			

1	BCOLD	**0**	R/W	V_{LTF_BOOST0} **(Typ. 76% of VREG or -10°C w/ 103AT thermistor)**	Set Boost Mode temperature cold monitor threshold voltage to disable boost mode
		1		V_{LTF_BOOST1} (Typ. 79% of VREG or -20°C w/ 103AT thermistor)	
0	FORCE_20PCT	**0**	R/W	**ICHG as Fast Charge Current (REG02[7:2]) and IPRECH as Pre-Charge Current (REG03[7:4]) programmed**	
		1		ICHG as 20% Fast Charge Current(REG02[7:2]) and IPRECH as 50% Pre-Charge Current (REG03[7:4])programmed	

PC/TC Control Register REG03, Address: 03 (Default Value: 00010001, or 11)

7:4	IPRECHG	0000	R/W	128mA	Pre-Charge Current Limit
		0001		**256mA**	
		0010		384mA	
		0011		512mA	
		0100		640mA	
		0101		768mA	
		0110		896mA	
		0111		1024mA	
		1000		1152mA	
		1001		1280mA	
		1010		1408mA	
		1011		1536mA	
		1100		1664mA	
		1101		1792mA	
		1110		1920mA	
		1111		2048mA	

3:0	ITERM	0000	R/W	128mA	Termination Current Limit
		0001		**256mA**	
		0010		384mA	
		0011		512mA	
		0100		640mA	
		0101		768mA	
		0110		896mA	
		0111		1024mA	
		1000		1152mA	
		1001		1280mA	
		1010		1408mA	
		1011		1536mA	
		1100		1664mA	
		1101		1792mA	
		1110		1920mA	
		1111		2048mA	

VCharge Control Register REG04, Address: 04 (Default Value: 10110010, or B2)

7:2	VREG		R/W	Binary	(V)	Binary	(V)	Binary	(V)	Binary	(V)
				0000 00	3.504	0100 00	3.760	1000 00	4.016	1100 00	4.272
				0000 01	3.520	0100 01	3.776	1000 01	4.032	1100 01	4.288
				0000 10	3.536	0100 10	3.792	1000 10	4.048	1100 10	4.304
				0000 11	3.552	0100 11	3.808	1000 11	4.064	1100 11	4.320
				0001 00	3.568	0101 00	3.824	1001 00	4.08	1101 00	4.336
				0001 01	3.584	0101 01	3.840	1001 01	4.096	1101 01	4.352
				0001 10	3.600	0101 10	3.856	1001 10	4.112	1101 10	4.368
				0001 11	3.616	0101 11	3.872	1001 11	4.128	1101 11	4.384
				0010 00	3.632	0110 00	3.888	1010 00	4.144	1110 00	4.400
				0010 01	3.648	0110 01	3.904	1010 01	4.16	1110 01	4.416
				0010 10	3.664	0110 10	3.920	1010 10	4.176	1110 10	4.432
				0010 11	3.680	0110 11	3.936	1010 11	4.192	1110 11	4.448
				0011 00	3.696	0111 00	3.952	**1011 00**	**4.208**	1111 00	4.464
				0011 01	3.712	0111 01	3.968	1011 01	4.224	1111 01	4.480
				0011 10	3.728	0111 10	3.984	1011 10	4.24	1111 10	4.496
				0011 11	3.744	0111 11	4.000	1011 11	4.256	1111 11	4.512
1	BATLOWV	0	R/W	2.8V						Pre-charge to fast charge	
		1		**3.0V**							
0	VRECHG	**0**	R/W	**100mV**						Battery recharge threshold	

		1		300mV	(below battery regulation voltage)
Charge Termination/Timer Control Register REG05, Address: 05 (Default Value: 10011010, or 9A)					
7	EN_TERM	0	R/W	Disable	Charging termination enable
		1		**Enable**	
6	TERM_STAT	**0**	**R/W**	**Match ITERM**	
		1		1 – STAT pin high before actual termination when charge current below 800 mA	
5:4	WATCHDOG	00	R/W	Disable timer	I^2C watchdog timer setting
		01		**40s**	
		10		80s	
		11		160s	
3	EN_TIMER	0	R/W	Disable	Charging safety timer setting
		1		**Enable**	
2:1	CHG_TIMER	00	R/W	5 hours	Fast charge timer setting
		01		**8 hours**	
		10		12 hours	
		11		20 hours	
0	Reserved	0		Reserved	
Boost Voltage/Thermal Regulation Control Register REG06, Address: 06 (Default Value: 01110011, or 0x73)					
7:4	BOOSTV	Binary	R/W	(V)	Output voltage of boost mode
		0000		4.550	
		0001		4.614	
		0010		4.678	
		0011		4.742	
		0100		4.806	
		0101		4.870	
		0110		4.934	
		0111		**4.998**	
		1000		5.062	
		1001		5.126	
		1010		5.190	
		1011		5.254	
		1100		5.318	
		1101		5.382	
		1110		5.446	
		1111		5.510	

3:2	BHOT	**00**	R/W	V_{HTF_BOOST0} **(36% of REG or 55°C w/ 103AT thermistor)**	Set Boost Mode hot temperature monitor threshold voltage to disable boost mode
		01		V_{HTF_BOOST1} (33% of REG or 60°C w/ 103AT thermistor)	
		10		V_{HTF_BOOST2} (30% of REG or 65°C w/ 103AT thermistor)	
		11		Disable boost mode thermal protection	
1:0	TREG	00	R/W	60°C	Thermal Regulation Threshold
		01		80°C	
		10		100°C	
		11		**120°C**	
Operation Control Register REG07, Address: 07 (Default Value: 01001011, or 4B)					
7	DPDM_EN	**0**	R/W	**Not in D+/D– detection**	Force DPDM detection. Back to 0 after detection complete.
		1		Force D+/D– detection when VIN power is presence	
6	TMR2X_EN	0	R/W	Safety timer not slowed by 2X during input DPM or thermal regulation	Safety Timer Setting during Input DPM and Thermal Regulation
		1		**Safety timer slowed by 2X during input DPM or thermal regulation**	
5	PPFET_Disable	**0**	R/W	**Allow PPFET turn on**	Force PPFET Off
		1		Turn off PPFET	
4	Reserved	0	R	0 – Reserved.	
3	Reserved	1		1 – Reserved.	
2	Reserved	0		0 – Reserved.	
1	INT_MASK[1]	0	R/W	No INT during CHRG_FAULT	
		1		**INT on CHRG_FAULT**	
0	INT_MASK[0]	0	R/W	No INT during BAT_FAULT	
		1		**INT on BAT_FAULT**	
System Status Register REG08, Address: 08					
7:6	VIN_STAT	00	R	Unknown (no input, or DPDM detection incomplete)	
		01		USB host	
		10		Adapter port	
		11		OTG	
5:4	CHRG_STAT	00	R	Not Charging	
		01		Pre-charge (<VBATLOWV)	
		10		Fast Charging	
		11		Charge Termination Done	
3	DPM_STAT	0	R	Not DPM	
		1		VINDPM or ILIMDPM	

2	PG_STAT	0	R	Not Power Good	
		1		Power Good	
1	THERM_STAT	0	R	Normal	
		1		In Thermal Regulation	
0	VSYS_STAT	0	R	Not in VSYSMIN regulation (BAT>VSYSMIN)	
		1		In VSYSMIN regulation (BAT<VSYSMIN)	
Fault Register REG09, Address: 09					
7	WATCHDOG_FAULT	0	R	Normal	Fault status
		1		Watchdog timer expiration	
6	OTG_FAULT	0	R	Normal	
		1		VIN overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that cannot start boost function)	
5:4	CHRG_FAULT	00	R	Normal	
		01		Input fault (VIN OVP or Bad source)	
		10		Thermal shutdown	
		11		Charge Safety Timer Expiration	
3	BAT_FAULT	0	R	Normal	
		1		BATOVP	
2	Reserved	**0**	R	Reserved	
		1			
1	NTC_FAULT[1]	0	R	Normal	
		1		Cold, Note: Cold temperature threshold is different based on device operates in buck or boost mode	
0	NTC_FAULT[0]	0	R	Normal	
		1		Hot, Note: Hot temperature threshold is different based on device operates in buck or boost mode	
Vender Info Register REG0A, Address: 0A					
7:5	PN	001	R	001 –HL7026	
4:3	Reserved	00	R	Reserved	
2:0	Reserved	000	R	Reserved	
Shipping Mode Register REG0B, Address: 0B					
7:3	Reserved	00000	R	Reserved	
2:0	TSHIP	**000**	R/W	**100ms**	Shipping mode activation delay
		001		9.1s	
		010		18.1s	
		011		27.1s	
		100		36.1s	

		101		45.1s	
		110		54.1s	
		111		63.1s	
IR Compensation / Boost Control Register REG0C, Address: 0C (Default Value: 00000000, or 00)					
7:5	BAT_COMP	**000**	R/W	**0mΩ**	IR Compensation Resister Setting
		001		10mΩ	
		010		20mΩ	
		011		30mΩ	
		100		40mΩ	
		101		50mΩ	
		110		60mΩ	
		111		70mΩ	
4:2	BAT_VCLAMP	**000**	R/W	**0mV**	IR Compensation Voltage Clamp (above regulation voltage)
		001		16mV	
		010		32mV	
		011		48mV	
		100		64mV	
		101		80mV	
		110		96mV	
		111		112mV	
1	Reserved	0	R	Reserved	
0	BOOST_9V_EN	**0**	R/W	**Disable 9V boost**	
		1		Enable 9V boost	
Misc Operation Register Control REG0D, Address:0D(default Value: 00010000, or 10)					
7	Reserved	0	R	Reserved	
6	DISABLE_TS	**0**	R/W	**TS1/TS2 functions enabled**	
		1		Disable TS1/TS2 detection	
5	VINDPM_OFFSET	**0**	R/W	**VINDPM thresholds are defined as REG00[6:3]**	
		1		VINDPM threshold defined in REG00[6:3] multiplied by 2.5	
4:0	Reserved	00000	R	Reserved	

Table 11 Register Bit Definitions

Application Information

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (4)$$

For best performance, VIN should be decoupled to PGND with at least 1μF effective capacitance. The remaining input capacitor should be place on VPRT. Also consider the voltage coefficients of the capacitor, which may reduce the effective capacitance from its rated value.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred because VIN can be as high as 20V during transients of the plug-in process, and any in-rush situation that may exist when external DC source has large AC components.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current ICOUT is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (5)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCF_{SW}^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation. To get good loop stability, The desired output capacitor range is 10uF to 20uF.

Output Inductor Selection

The HL7026 has 1.5 MHz switching frequency to allow the use of small 1uH inductor. The Inductor saturation current should be higher than the charging current (I_{CHG}, 3A) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \quad (7)$$

The inductor ripple current depends on input voltage (V_{VIN}), duty cycle (D = V_{BAT}/V_{VIN}), switching frequency (F_{SW}) and inductance (L):

$$I_{RIPPLE} = \frac{V_{VIN} \times D \times (1 - D)}{F_{SW} \times L} \quad (8)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design. Typical inductor value is 1μH.

PCB Layout Reference

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 31) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to VPRT pin and PGND pin connections and use shortest copper trace connection or PGND plane.

2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.

4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or use a 0Ω resistor to tie analog ground to power ground.

5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.

6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.

7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

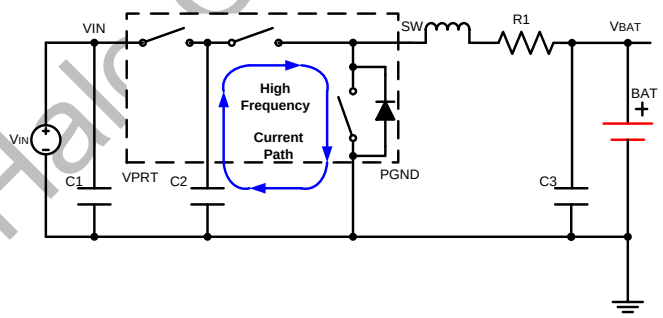
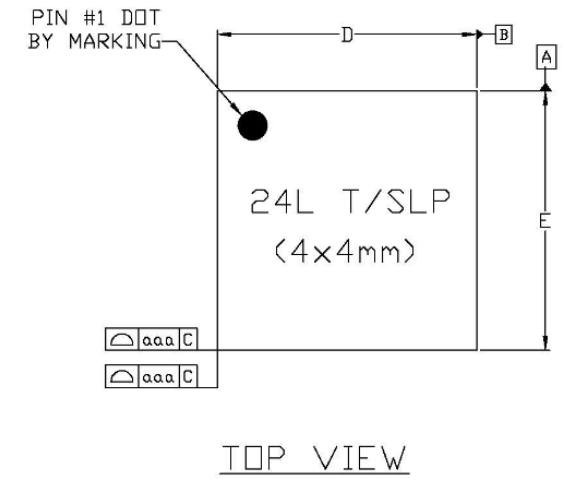
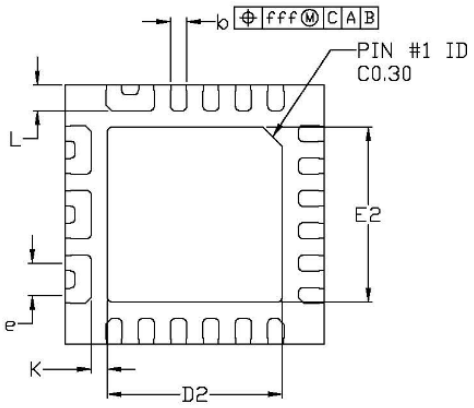


Figure 31 High Frequency Current Path

Package Information

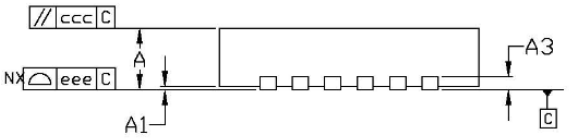


TOP VIEW



BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	0.750	0.800
	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	3.950	4.000	4.050
E	3.950	4.000	4.050
D2	2.650	2.700	2.750
E2	2.650	2.700	2.750
--	--		
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450
K	0.25 Ref.		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

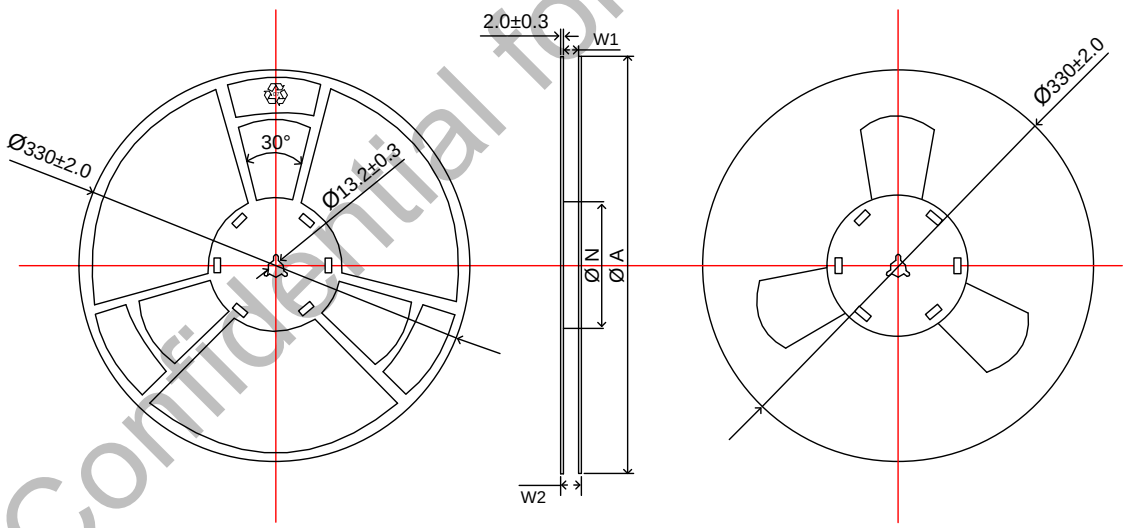


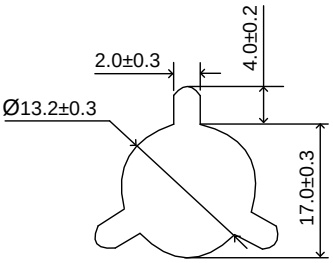
SIDE VIEW

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

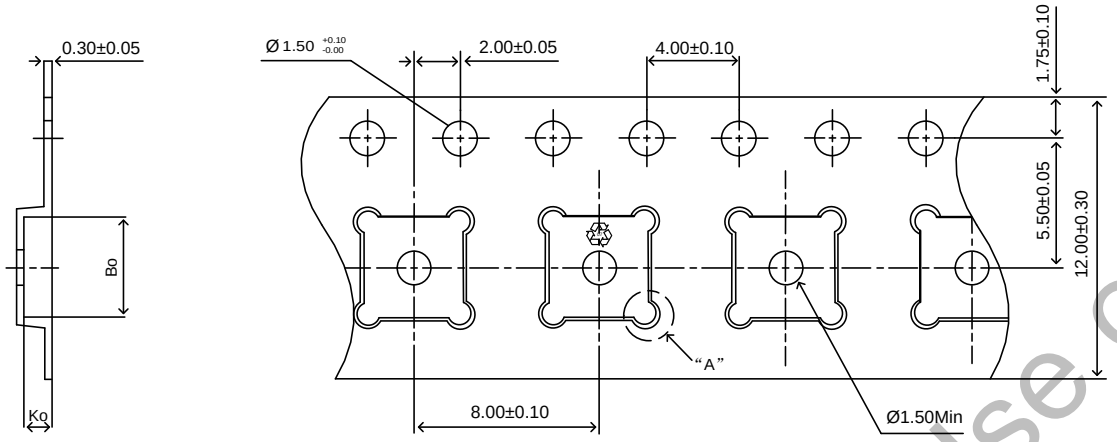
Tape and Reel Information





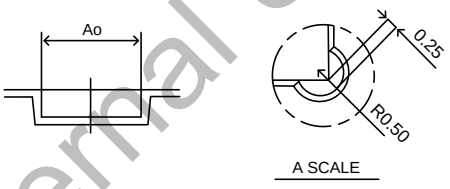
PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1(Min)	W2(Max)
12MM	330±2.0	100±1.0	12.4	19.4

Reel Information



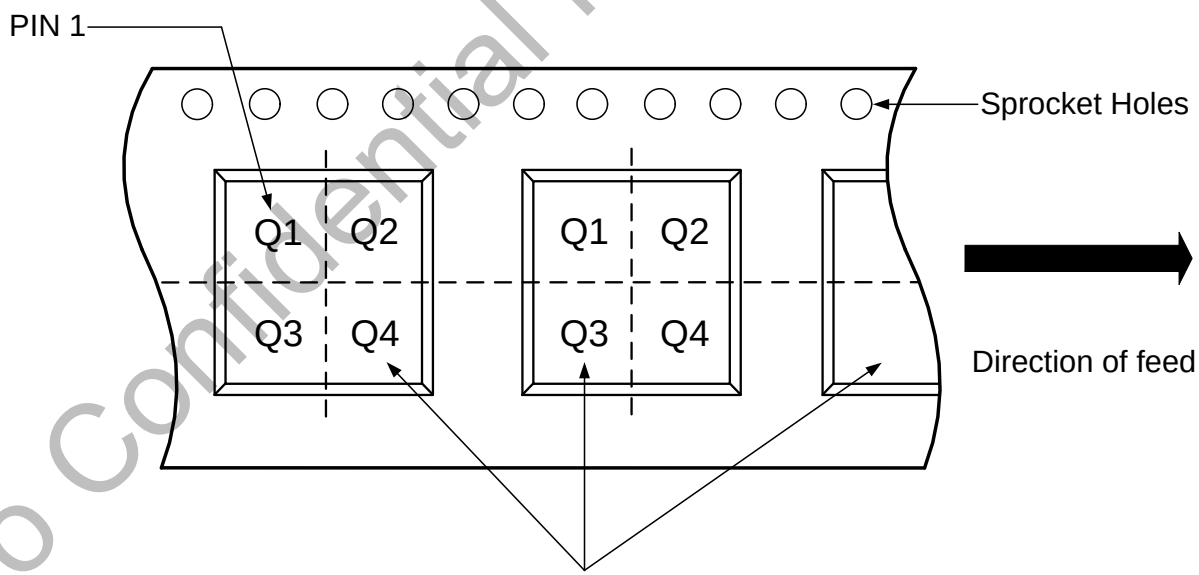
NOTE:

1. *10 sprocket hole pitch cumulative toterance 0.2/-0.2*
2. *Camber not to exceed 1mm in 250mm*
3. *Material: Black conductive Polystyrene*
4. *Ao and Bo measured on a plane 0.3mm above the bottom of the pocket*
5. *Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier*
6. *Pocket center position relative to sprocket hole center measured as true position center of pocket, not pocket hole center*
7. *Pocket center and pocket hole center must be same position*



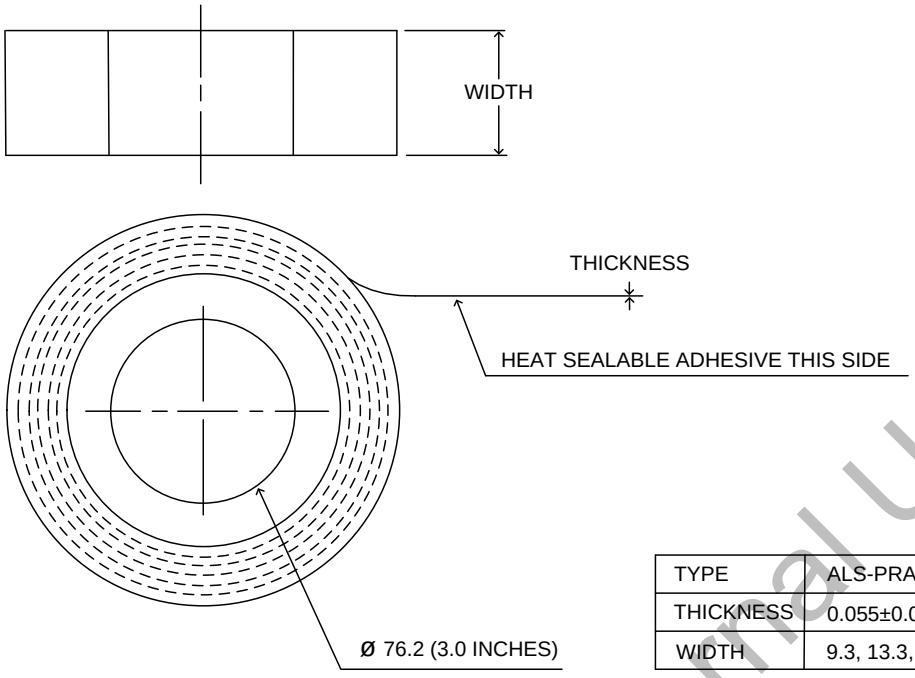
Ao	4.30±0.10
Bo	4.30±0.10
Ko	1.10±0.10
K1	–

Carrier Tape Information



Pocket Quadrants

PIN 1 Orientation in Tape



TYPE	ALS-PRA
THICKNESS	0.055±0.01
WIDTH	9.3, 13.3, 21.3±0.10

NOTE:
1. MATERIAL: ANTISTATIC POLYESTER FILM
2. COLER: TRANSPARENT, PALE BLUE

Cover Tape Information

Important Notice

Halo Micro reserves the right to modify, improve and terminate its products, service, documentation, etc. without advance notice. Customers are encouraged to contact Halo Micro sales representative get the latest product information.

Without proper legal authorization, Halo Micro products shall not be used for medical or military applications. Halo Micro does not assume any liability of personal or property damages of any kind due to such applications.

All text, images, trademarks of this document, and any intellectual property contained in the product and in this document belong to Halo Micro No part of this document may be used, copied, modified, distributed or published without legal authorization from Halo Micro.